WHAT IS CLAIMED IS:

1. A mixer circuit, comprising:

a signal input;

an RF transconductance circuit that is configured to convert an input differential signal received at said signal input to a differential current, said RF transconductance circuit having a pair of field effect transistors;

a LO switching circuit configured to switch said differential current between outputs of said mixer circuit at a rate determined by a differential LO signal; and

means for adding DC current to said pair of field effect transistors in said RF transconductance circuit.

2. The mixer circuit of claim 1, wherein said means for adding DC current includes at least one current source configured to generate said DC current.

3. The mixer circuit of claim 2, wherein said current source is a variable current source.

4. The mixer circuit of claim 3, wherein said variable current source adjusts said DC current so as to reduce flicker noise in the mixer circuit.

5. The mixer circuit of claim 1, wherein said DC current bypasses said LO switching circuit.

6. A mixer circuit , comprising:

a signal input;

an RF transconductance circuit having a pair of field effect transistors (FETs) that are configured to convert an input differential signal received at said signal input to a differential current;

a LO switching circuit configured to switch said differential current between outputs of said mixer circuit at a rate determined by a differential LO signal;

a first current source configured to add a first DC current to a first FET of said pair of FETs; and

a second current source configured to add a second DC current to a second FET of said pair of FETs.

7. The mixer circuit of claim 6, wherein said first current source is a variable current source that adjusts said first DC current to minimize flicker noise of said mixer circuit.

8. The mixer circuit of claim 6, wherein said second current source is a variable current source that adjusts said second DC current to minimize flicker noise of said mixer circuit.

9. The mixer circuit of claim 6, wherein said first DC current and said second DC current bypass said LO switching circuit.

10. The mixer circuit of claim 6, wherein said first DC current is added to a drain of said first FET in said pair of FETs, and said second DC current is added to a drain of said second FET in said pair of FETs.